CLAIM SET AS AMENDED

1. (Currently Amended) A method for forming a capacitor of a semiconductor device comprising the steps of:

forming a first insulation layer on the upper surface of a semiconductor substrate;

forming a second insulation layer on the upper surface of the first insulation layer;

forming a third insulation layer on the upper surface of the second insulation layer;

etching a predetermined depth of the third insulation layer over a first region of the semiconductor substrate so that a thickness of the third insulation layer over the first region is thinner than a thickness of the third insulation layer over a second region of the semiconductor substrate;

sequentially etching the third insulation layer and the second insulation layer to form at least one hole over ~~a first~~ **the second** region of the semiconductor substrate;

forming a conductive layer over the semiconductor substrate;

performing Chemical Mechanical Polishing (CMP) until an upper surface of the third insulation layer is exposed; and

removing portions of the third insulation layer from the ~~first~~ **second** region.

2. (Original) The method according to claim 1, wherein the second and the third insulation layers have different etching characteristic with respect to each other.

3. (Original) The method according to claim 2, wherein the second insulation layer is made of a nitride.

4. (Original) The method according to claim 2, wherein the third insulation layer is made of an oxide.

5. (Original) The method according to claim 1, wherein the first insulation layer is made of an oxide.

6. (Cancelled)

7. (Currently Amended) The method according to claim ~~6~~ 1, wherein the depth is 100Å ~ 2000Å.

8. (Currently Amended) The method according to claim ~~6~~ 1, after the etching a predetermined depth step and prior to the sequentially etching step, further comprising a step of:

forming a hard-masking thin film on the upper surface of the third insulation layer; and

patterning the hard-masking thin film to form a hard mask.

9. (Original) The method according to claim 8, wherein the hard-masking thin film is made of polycrystalline silicon.

10. (Currently Amended) The method according to claim 8, wherein the hard mask formed on the upper surface of the third insulation layer over the ~~second~~ **first** region remains after the performing CMP step.

11. (Currently Amended) The method according to claim 1, wherein the sequentially etching step further forms a line along a boundary between the first region and a second region of the semiconductor substrate by removing **portions of** the third insulation layer and of the second insulation layer.

12. (Original) The method according to claim 1, wherein the conductive layer is made of polycrystalline silicon.

13. (Original) The method according to claim 1, wherein the removing step is performed using a wet station.

14. (Previously Presented) The method according to claim 13, wherein the wet station is a bath type.

15. (Previously Presented) The method according to claim 13, wherein the wet station employs an IPA vapor drier.

16. (Currently Amended) The method of claim 1, prior to the sequentially etching step, further comprising:

forming a hard mask film on the third insulation film;

forming a photoresist pattern on the hard mask film; and wherein

the sequentially etching step etches the hard mask film using the photoresist pattern as a mask and etches the third and second insulation layers using the etched hard mask film and the ~~**photo resist**~~ **photoresist** pattern.

17. (Original) The method of claim 1, wherein the performing CMP step forms non-sharp upper edges of the conductive layer.

18. (Original) The method of claim 1, wherein the removing step further removes slurry material from the first region.

19. (Cancelled)

20. (Original) A method for forming a capacitor of a semiconductor device comprising the steps of:

forming a first insulation layer on the upper surface of a semiconductor substrate;

forming a second insulation layer on the upper surface of the first insulation layer;

forming a third insulation layer on the upper surface of the second insulation layer;

etching the third insulation layer over a peripheral portion of the semiconductor substrate;

forming a hard mask film over the third insulating layer;

forming a photoresist pattern on the hard mask film;

sequentially etching the hard mark film, the third insulation layer and the second insulation layer to form at least one hole over a first region of the semiconductor substrate;

forming a conductive layer over the semiconductor substrate;

performing Chemical Mechanical Polishing (CMP) until an upper surface of the third insulation layer is exposed; and

removing portions of the third insulation layer from the first region.